1. In Accessing the word file ------------ locality of reference is used.
2. Temporal, b-Spatial, c- Sequential, d- incremental
3. Accessing the array elements ------------ locality of reference is used.
4. Temporal, b-Spatial, c- Sequential, d- incremental
5. I f there is a read miss occurred in virtual address cache and sufficient space is available in cache,
6. Virtual address is used to transfer data from main memory to cache memory.
7. Virtual address is used to transfer data from cache memory to main memory.
8. Virtual address is translated into physical address and this physical address is used to transfer data from main memory to cache memory.
9. Virtual address is translated into physical address and this physical address is used to transfer data from cache memory to main memory.
10. If the size of main memory (MM) is 32 bit, cache memory (CM) size is 16 bit, and memory is byte addressable then the capacity of main memory and cache memory are
    1. MM 232 bytes and CM 216 bytes
    2. MM 224 byte and CM 28 bytes
    3. MM 232 words and CM 216 words
    4. MM 224 words and CM 28 words
11. Let suppose associative mapping is used on the above memory hierarchy (Q.4) then how many bits will be used in tag field if block size is 4 byte.
    1. 22 bits, b. 24 bits, c. 32 bits d. 30 bits
12. In 4-way interleaved memory (4 memory modules with 16 word each), how would you translate the memory address?
    1. First 4 bit for word and last 2 bit for module
    2. First 2 bit for word and last 4 bit for module
    3. First 2 bit for module and last 4 bit for word
    4. First 4 bit for module and last 2 bit for word
13. Memory Inclusion property states that “ The data across all the memory levels (M0, M1-----Mn) should be consistent”.
    * 1. a-True, b-False
14. If 36 control signals are required in a processor system, the number of bits required to encode them in a strictly vertical organization will be:
    1. 5 6 7 8
15. A control signal Y is generated in the T4 stage for an instruction I1, T3 stages for instructions I2 and I3 and T2 stage for instruction I4. How many AND gates will be required for hardware generation of this signal?
    1. 1 2 3 4
16. A non-pipelined system has four stages taking times 3 ns, 4 ns, 5ns and 5 ns respectively. What should be the clock frequency (in MHz) if this is converted into a pipelined system?
    1. 200 250 300 350
17. For a 1024\*16 SRAM chip, how many external connections will be required?
    1. 16 24 28 30
18. Consider two instructions (first operand represents destination) in a 5-stage pipeline:
    1. ADD R5, R2, #30
    2. SUB R5, R2, #40
    3. Which possible data hazard is present (if any)?
    4. RAW WAR WAW None
19. At the time the instruction Load R6, 1000(R9) is fetched, R6 and R9 contain the values 4200 and 85320, respectively. Memory location 86320 contains 75900. What will be the content of interstage register RZ after stage 3 execution step of this instruction.
    1. 4300 86320 75900 4200
20. Assume that a multiprocessor has eight processors. Based on an existing program that runs on one processor, a parallel program is written to run on this multiprocessor. Assume that the workload of the parallel portion of the program can be distributed evenly over the eight processors. Use Amdahl’s Law to compute the fraction of the parallel program that allows a speedup of 5.
    1. 0.91 0.19 0.83 None of these
21. What will be the ideal CPI of a 5-stage pipelined processor with clock speed 200 MHz?
    1. 5 0.5 1 0.2
22. Consider the addition of -7 and +3, determine which of the following condition code flags are set:
    * + 1. Carry (C)
        2. Overflow (V)
        3. Zero (Z)
        4. Sign (N)
23. Assume that program is stored in the byte addressable memory with start address of 200 and word size is 32-bits. During the execution of instruction I3 what could be the value present in program counter (PC)?
    * + 1. 2016
        2. 2012
        3. 2015
        4. 2017
24. -----------------------addressing mode is an efficient way to access linear array elements
    * + 1. Register Addressing Mode
        2. Auto indexed Addressing Mode
        3. Immediate Addressing Mode
        4. Indirect Addressing Mode
25. If a computer system has 612 no. of instruction then how many bits are required to represent opcode field of an instruction format?
    * + 1. 9 bits
        2. 10 bits
        3. 8 bits
        4. 7 bits
26. Examine the following statements:

I: RISC supports variable length of instruction

II: A compiler has to do lot of work in RISC style.

III: In RISC style, instruction-decoding logic is complex

which of the following is TRUE about RISC Computer?

* + - 1. I, II and II are true
      2. I, II and II are false
      3. I, III are false but II is true
      4. I, II are true but III is false

1. Instruction decode (ID) unit:
   * + 1. determines total number of operations
       2. identifies type of operation
       3. specifies addressing mode
       4. none
2. In which addressing mode, the address field of instruction gives the address of memory location where the effective address is stored.
   * + - 1. Displacement Addressing Mode
         2. Immediate Mode
         3. Direct Addressing Mode
         4. Indirect Addressing Mode
3. Task of linker is/are

I: translate source code into object code

II: combine all object module to a complete image

III: resolve external & internal references

* + - 1. I & II
      2. II & III
      3. I & III
      4. I, II & III

1. Mark the false statement for Assembler Directives:

I: An instruction that will be executed when the object program is run

II: It does not appear in the object program

* + - 1. Only I
      2. Only II
      3. Both false
      4. None

1. The smallest integer that can be represented by a 9-bit number in 2’s complement form is:  
   (a) -255  
   (b) -256  
   (c) -127

(d) 0

1. Consider a machine supports 2-address instructions, a 24-bit instruction is placed in a word-addressable memory consisting of 128 words. The number of possible operations is?  
   (a) 1024  
   (b) 512  
   (c) 128

(d) 2048

1. Result of subtraction of -5 from -7 in the 2’s-complement system:
   * + 1. 1 1 1 0
       2. 1010
       3. 1101
       4. 1011
2. Example of Immediate addressing mode:
   * + 1. Add R2,R1
       2. Add R2, #5
       3. Add R2, 100(R3)
       4. Add R5, (R2+R3)
3. To resolve the forward reference problem in assembly process, we use :
   * + - 1. Loader  
            b) Two-pass assemblerc) Op-Assembler  
            d) Debugger
4. How many address bits are required to represent 256 G memory:
   * + - 1. 38bits
         2. 18bits
         3. 48 bits
         4. 8bits
5. Array processor is an example of:
   * + - 1. SISD Architecture
         2. MIMD Architecture
         3. SIMD Architecture
         4. MISD Architecture
6. **.** -------------------Register is used to hold the currently fetched instruction to decode
   * + - 1. Memory Buffer Register
         2. Memory Address Register
         3. Instruction Register
         4. Program Counter
7. Status of memory is given below.
   1. word 100 contains 300
   2. word 200 contains 400
   3. word 300 contains 600
   4. word 400 contains 700

Which of the following instruction is used to load 600 into the accumulator?

* + - 1. load immediate 300
      2. load indirect 400
      3. load immediate 100
      4. load indirect 100

1. For the instruction MOVE R3, R7, how many times will the memory be accessed?
   * + - 1. 0
         2. 1
         3. 2
         4. 3
2. In the instruction LOAD R3, 100(R1), what will be the effective memory address from where the operand is fetched? Assume, R1 currently holds 2500 and R3 holds 3000. Also instruction is present at memory address 1000.
   * + - 1. 1000
         2. 2500
         3. 2600
         4. 3000